Design of a Bit Interleaver for the High-order Constellation DVB-T2 System

Inwoong Kang, Kyu-Soon Ok, Youngmin Kim, Jae Hyun Seo, Heung Mook Kim, Member, IEEE, and Hyoung-Nam Kim, Member, IEEE

Abstract—Since the DVB-T2 system provides high spectral efficiency among commercialized digital terrestrial transmission (DTT) systems, it has been considered as a prospective option for the base system of next generation DTT systems providing UHDTV service. However, when the high order modulation scheme such as 1024-QAM is employed, a bit interleaver in DVB-T2 should be newly designed. The design of a bit interleaver aims to improve the decoding performance not only by obtaining time diversity gain but also by eliminating multi-edge symbols. Although there are a few literatures about the design of a bit interleaver exploiting the multi-edge elimination, they cannot be directly applied to the bit interleaver of the DVB-T2 because they work as a group with a bit-to-cell demultiplexer. In this respect, this paper presents a bit interleaver design procedure for the high-order constellation DVB-T2 system. The proposed procedure generates bit interleavers for any modulation orders and makes it possible that a newly designed bit interleaver performs multi-edge elimination with all the LDPC code rates. Simulation results show that a newly designed bit interleaver for 1024-QAM achieves about 0.6dB SNR gain over a random interleaver under a Rayleigh fading channel.

Index Terms—Bit interleaver, DVB-T2, High-order modulation, UHDTV

I. INTRODUCTION

Since ultra-high definition television (UHDTV) standard is expected to require much greater transmission data rate than the high definition television (HDTV) standard, the main consideration of the development of the next generation digital terrestrial transmission (DTT) system for UHDTV lies in increasing the transmission data rate of the conventional DTT system. As one prospective method for achieving higher data rate, high-order constellation schemes such as 1024-QAM and 4096-QAM have been studied [1]. In particular, the digital video broadcasting-2nd generation terrestrial (DVB-T2) system may be considered as one of the most effective base systems for such high-order constellation schemes to be adopted because of its superior spectral efficiency [2].

When such high-order constellations are adopted into the DVB-T2 system, the bit interleaver should be newly designed. In designing a bit interleaver, eliminating multi-edge symbols must be considered in addition to achieving time diversity [3]. By eliminating the multi-edge symbols via a bit interleaver, it is shown that the decoding performance can be significantly improved [3]. Although there are a few literatures about the design of a bit interleaver performing the multi-edge elimination, they cannot be directly applied to the DVB-T2 system because the bit interleaver operates in cooperation with a bit-to-cell demultiplexer before the interleaved codeword is modulated. In this respect, we present a design procedure of the DVB-T2 bit interleaver. By the proposed procedure, we generate a bit interleaver for any modulation orders including high-order modulation schemes. The generated bit interleaver performs the multi-edge elimination with all LDPC code rates.

The rest of this paper is organized as follows: In section II, the BICM structure of the DVB-T2 system is described. The proposed design procedure of a bit interleaver is presented in section III with the corresponding simulation results. Conclusion is given in section IV.

II. BICM OF THE DVB-T2 SYSTEM

A block diagram of the DVB-T2 system is depicted in Fig. 1. Bit-interleaved coded modulation (BICM) of the DVB-T2 system consists of an LDPC encoder, a QAM mapper and a bit mapper. Output symbols of the QAM mapper are symbol-wise interleaved before being OFDM-modulated. Unlike the general BICM system using a bit interleaver between a channel encoder and a modulator, the DVB-T2 employs two blocks: a bit interleaver and a bit-to-cell demultiplexer (DEMUX).

The bit interleaver of the DVB-T2 system scrambles bits in...
one input codeword via a block interleaver as described in Fig. 2. The figure shows that the input codeword is written in a column-wise direction and then read in a row-wise direction. The bit interleaved codeword is divided into $N$ sub-streams, $v_i$, and the bit-to-cell DEMUX reorder $v_i$ with a new ordering sequence, $e$, defined by the bit-to-cell DEMUX:

$$u_i = v_{e(i)}, \quad i = 1, 2, \ldots, N$$

(1)

where $u_i$ denotes the reordered sub-stream. When the codeword is written in a column-wise manner, the twisting factor $t_c$ determines all offset points where writing starts in each column. The main role of the twisting factor is to adjust the block interleaving so that the interleaved codeword does not have the multi-edge symbols. Since the modulation order defines the number of columns of the interleaving block, the twisting factor is designed according to the modulation order as well as the channel code rate. In this respect, the design of the bit interleaver of the DVB-T2 system mainly lies in determining the twisting factor for a certain modulation order, and the DVB-T2 specification requires for the interleaver to work with all included LDPC codes with different code rates. In the following section, we propose a bit interleaver design algorithm working with all LDPC code rates.

III. DESIGN OF A BIT INTERLEAVER

As mentioned in the previous section, the design of a bit interleaver is led to the design of a twisting factor. Fig. 3 presents a flowchart of the proposed design procedure of a bit interleaver. The circular shifting of $N$ divided sub-streams of the codeword is expressed as a circular shifting by the twisting factor $t_c$ of $N$ divided $N_{\text{column}} \times N_{\text{row}}$ sub parity check matrices (PCM). The twisted sub PCMs are then accumulated to a summation matrix $S$:

$$S = \sum_{i=1}^{N} H_i$$

$$= \sum_{i=1}^{N} \left[ H_{N_{\text{column}} \times (i-1)+1 \cdot N_{\text{column}}} \ H_{N_{\text{column}} \times (i-1)+1 \cdot N_{\text{column}}} \right]$$

(2)

where $H_{ij}$ denotes the sub matrix having from $i$th to $j$th columns of the parity check matrix $H$. The ones in the sub PCM $H_i$ denote the edges between the $i$th bit in a modulated symbol and the corresponding parity check equations. Therefore, the nonzero elements of the summation matrix $S$ mean the number of edges in modulated symbols.

The summation matrix $S$ is used for the design of a bit interleaver as described in Fig. 2. The figure shows that the input codeword is written in a column-wise direction and then read in a row-wise direction. The bit interleaved codeword is divided into $N$ sub-streams, $v_i$, and the bit-to-cell DEMUX reorder $v_i$ with a new ordering sequence, $e$, defined by the bit-to-cell DEMUX:

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Table I NEWLY DESIGNED BIT INTERLEAVER TWISTING FACTOR

<table>
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<tr>
<th>Modulation</th>
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<tr>
<td>1024-QAM</td>
<td>$[0 \ 1 \ 3 \ 5 \ 6 \ 9 \ 12 \ 15 \ 16 \ 19 \ 21 \ 23 \ 25 \ 28 \ 28]$</td>
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where $H_{ij}$ denotes the sub matrix having from $i$th to $j$th columns of the parity check matrix $H$. The ones in the sub PCM $H_i$ denote the edges between the $i$th bit in a modulated symbol and the corresponding parity check equations. Therefore, the nonzero elements of the summation matrix $S$ mean the number of edges in modulated symbols.

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TABLE II
SIMULATION PARAMETERS

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<thead>
<tr>
<th>Parameters</th>
<th>Specifications</th>
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<tbody>
<tr>
<td>Bandwidth</td>
<td>6 MHz</td>
</tr>
<tr>
<td>Elementary period</td>
<td>7/48 μs</td>
</tr>
<tr>
<td>FFT size</td>
<td>32 K</td>
</tr>
<tr>
<td>Guard interval</td>
<td>1/128</td>
</tr>
<tr>
<td>Modulation</td>
<td>1024-QAM</td>
</tr>
<tr>
<td>LDPC code rate</td>
<td>1/2, 3/5, 2/3, 3/4, 4/5, and 5/6</td>
</tr>
</tbody>
</table>

TABLE III
BIT-TO-CELL DEMUX REORDERING SEQUENCES WITH VARIOUS CODE RATES

<table>
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<tr>
<th>MODULATION</th>
<th>Code rate (R)</th>
<th>ε</th>
</tr>
</thead>
<tbody>
<tr>
<td>1024-QAM</td>
<td>1 (1/2)</td>
<td>[2 6 4 5 8 1 3 10 7 9]</td>
</tr>
<tr>
<td></td>
<td>2 (3/5)</td>
<td>[4 5 6 10 8 3 2 9 7 1]</td>
</tr>
<tr>
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<td>3 (2/3)</td>
<td>[9 3 10 8 1 4 5 2 6 7]</td>
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interleaver. The proposed design method produces a twisting factor $t_c$ that results in a summation matrix with no element bigger than one. In addition, the design method generates a twisting factor $t_c$ for the parity check matrices of all the LDPC code rates. By the proposed design algorithm, the newly designed bit interleaver twisting factor is given in Table I. The designed twisting factor is a vector of length 20 which is a double of the modulation order. Each element in $t_c$ denotes the starting point of the circular shift of the divided sub PCMs, resulting in no multi-edge symbols at the QAM mapper output.

The performance improvement using the newly designed bit interleaver was verified by simulation results in Figs. 4 and 5. The bit-error rate (BER) performances were extracted in the simulation parameter set in Table II. As simulation parameters, the 6MHz bandwidth and the corresponding 7/48 us of the elementary period were considered. The FFT size and the guard interval were 32K and 1/128, respectively in order to reduce the overhead. In particular, the 1024-QAM modulation scheme was tested with 6 different LDPC code rates over an AWGN channel and a statistically modeled TU-6 channel.

The simulation results verify that the decoding performance of the DVB-T2 system can be significantly improved by using the bit interleaver. In Figs. 4 and 5, the BER curves over the AWGN channel and the TU-6 statistical channel are plotted. BER curves with different code rates are distinguished by the markers on the curves, where BM and RI stand for the bit mapper and the random interleaver. Each figure shows that the BER performance has about 0.6 dB SNR improvement with the newly designed bit interleaver (BER curves with solid markers) compared to the performance without any bit interleaver (BER curves with open markers). Moreover, the BER performance with random interleavers (dashed line) exhibits smaller amount of performance improvement because the multi-edge symbols are generated. Meanwhile, the 1024-QAM bit-to-cell DEMUX with various channel code rates were also given in Table III according to [4] because the bit interleaver works in cooperation with the bit-to-cell DEMUX.

IV. CONCLUSION

A design method for the bit interleaver of the DVB-T2 system is proposed. It was shown that the newly designed bit interleaver for 1024-QAM modulation results in a significant performance improvement compared to a random interleaver. As the future digital transmission system is expected to employ high-order modulation schemes, it is expected that the proposed bit interleaver design method may be used for the development of the next generation DTT system. Especially for the future DTT system, the proposed bit interleaver design may be further advanced in the MIMO structure.

REFERENCES

In-Woong Kang received the BS degree in electronic and electrical engineering from Pusan National University (PNU), Busan, Korea, in 2011. He is currently working toward the PhD degree at the Communications and Signal Processing Laboratory (CSPL), Department of Electronics Engineering at Pusan National University, Busan, Korea. His research interests are in the area of digital signal processing, MIMO-OFDM systems, in particular, signal processing for digital broadcasting, and digital communications.

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